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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/556,607	04/21/2000	Arthur Joseph Kalb	135469-200200 (P04342)	6834

7590 10/19/2004

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/556,607	KALB, ARTHUR JOSEPH	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to RCE filed on 7/29/04 in which claims 1-57 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tripathi et al U.S. Patent No 5,974,089 in view of Beard U.S. patent No 5,796,359.

As per claims 1, 20 and 39 Tripathi et al discloses an apparatus including a circuit for converting an analog signal to a pulse width modulated signal comprising: an integration stage (see fig. 3 elements 302 or 306 and col.6, lines 7-11) configured to receive combine and integrate an analog input signal and a set of one or more feedback signals and in accordance therewith provide a set of one or more integrated signals; a modulation stage, (see fig.3 element 300, and col.5, lines 9-35 and col.6, line 6) coupled to said integration stage, configured to receive and modulate a final portion of said set of one or more integrated signals and in accordance therewith provide a time pulse width modulation (see col.1, lines 18-19 and col.6, lines 13-25); a first feedback stage (see fig.3 and abstract and col.5, lines 28-37 and col.6, lines 20-25), coupled between said modulation stage and said integration stage, configured to receive said time pulse width

modulation (see abstract) in accordance therewith provide a first portion of said set of one or more feedback signals.

However Tripathi does not teach a first feedback to receive discrete time pulse width modulation.

Beard teaches providing discrete time (see figs. 1-2 and col.2, line 8 and col.3, lines 23-67 and col.4, lines 5-67) pulse and said modulation stage and said integration stage, configured to receive said discrete time pulse width modulation.

It would have been obvious to one of ordinary skill in the art to implement the discrete time of Beard into Tripathi as for the magnitude of the analog feedback signal produced by the feedback filter to be proportional to the width of the pulses of the digital feedback produced by the PWM as taught by Beard (see col.4, lines 15-18).

As per claims 2, 21 and 40 the apparatus of Tripathi does include an adder and an integration stage to provide a first combined signal (see fig.3 element 304).

As per claims 3, 22 and 41 the apparatus of Tripathi would include a feed forward circuit as to accurately analyze the modulator by modeling ideal quantization noise and other sources of non-ideal noise introduced by the feed forward ADC converter.

As per claims 4, 23 and 42 the apparatus of Tripathi does include a continuous integration stage (see col.6, lines 18-23).

As per claims 5, 24 and 43 the apparatus of Tripathi does include at least one sampled integrator circuit (see fig.3).

As per claims 6, 7, 25, 26 and 44-45 Tripathi does include a quantization stage (se col.1, lines 33-42 and col.5, lines 41-45).

As per claims 8, 27 and 46, the Tripathi and Bear in combination would include a discrete time Pulse width modulation stage to receive at least one digital input signal as for the magnitude of the analog feedback signal produced by the feedback filter to be proportional to the width of the pulses of the digital feedback produced by the PWM as taught by Beard (see col.4, lines 15-18).

As per claims 9, 28 and 47-49 the apparatus of Tripathi does include a continuous integration stage (see col.6, lines 18-23).

As per claim 10, the apparatus Tripathi and Bear in combination would include a first feedback stage having a discrete time as for the magnitude of the analog feedback signal produced by the feedback filter to be proportional to the width of the pulses of the digital feedback produced by the PWM as taught by Beard (see col.4, lines 15-18).

As per claims 11, 29-30, Tripathi and Bear in combination would include a first feedback stage having an anti-aliasing stage to filter said discrete time pulse width modulation as for the magnitude of the analog feedback signal produced by the feedback filter to be proportional to the width of the pulses of the digital feedback produced by the PWM as taught by Beard (see col.4, lines 15-18).

As per claims 12, 31 and 50 the apparatus of Tripathi does include a second feedback stage and a quantization stage and an integration stage (see fig.3).

As per claims 13, 32 and 51 the apparatus Tripathi does include an integration stage having a first and second adders (see fig.3).

As per claims 14, 33 and 52 the apparatus of Tripathi does include a continuous integration stage (see col.6, lines 18-23).

As per claims 15, 16, 34-35 and 53-54 Tripathi and Bear in combination would include a quantization stage in accordance with a discrete time Pulse width modulation stage as for the magnitude of the analog feedback signal produced by the feedback filter to be proportional to the width of the pulses of the digital feedback produced by the PWM as taught by Beard (see col.4, lines 15-18).

As per claims 17, 36 and 55, Tripathi and Bear in combination would include a discrete time Pulse width modulation stage to receive at least one digital input signal as for the magnitude of the analog feedback signal produced by the feedback filter to be proportional to the width of the pulses of the digital feedback produced by the PWM as taught by Beard (see col.4, lines 15-18).

As per claims 18, 37 Tripathi and Bear in combination would include a first feedback having a continuous time feedback and a second feedback having a discrete time feedback as for the magnitude of the analog feedback signal produced by the feedback filter to be proportional to the width of the pulses of the digital feedback produced by the PWM as taught by Beard (see col.4, lines 15-

18a first feedback stage having a continuous integration stage (see col.14, lines 58-67).

As per claims 19, 38 and 56-57 the apparatus of Tripathi does include a first feedback stage and a second feedback stage and a filter (see fig.3).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Melanson U.S. patent No 6,414,614 B1 teaches a power output stage compensation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

EMMANUEL BAYARD
PRIMARY EXAMINER

October 15, 2004